4/2000
4/2001

IN THE CLAIMS:

Claims 1-30. (Cancelled).

31. (Currently Amended) A method of manufacturing ~~method of~~ a semiconductor device including ~~a CMOS circuit formed by~~ an n-channel TFT and a p-channel TFT comprising the steps of:

~~a process of~~ forming a first wiring line on a substrate,

~~a process of~~ forming a first insulating layer on the first wiring line,

~~a process of~~ forming an active layer of the n-channel TFT and an active layer of the p-channel TFT on the first insulating layer, wherein the active layer of the n-channel TFT is located over the first wiring line with the first insulating film interposed therebetween and the active layer of the p-channel TFT does not overlap any portion of the first wiring line,

~~a process of~~ forming a second insulating layer ~~by overlapping~~ on the active layer of the n-channel TFT and the active layer of the p-channel ~~layer~~ TFT, ~~and~~

~~a process of~~ forming a second wiring line on the second insulating layer, and

~~a process of~~ forming a LDD region ~~on~~ in the active layer of the n-channel TFT; ~~and~~

wherein the LDD region is provided ~~overlap~~ overlapping the first wiring line and not ~~to overlap~~ overlapping the second wiring line.

32. (Currently Amended) ~~Manufacturing~~ The method of manufacturing ~~a~~ the semiconductor device according to claim 31, ~~characterized in that~~

wherein each of the first wiring line and~~! or~~ the second wiring line is ~~formed by~~ made of a conductive film ~~mainly~~ containing an element selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si)~~, or an alloy film or silicide film containing the above elements in combination~~.

33. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over said the first ~~gate electrode~~ wiring line with ~~said~~ the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a first channel region therebetween;

forming at least one second N-type impurity region between the first channel region and the first N-type impurity regions, wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in ~~said~~ the first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a second channel region therebetween;

forming a second insulating film over said the first semiconductor island and the second semiconductor ~~islands~~ island; and

forming a second ~~gate electrode~~ wiring line over the first channel region of the first semiconductor island and a third ~~gate electrode~~ wiring line over the second channel region of the second semiconductor island,

wherein there is an overlap between the first ~~gate electrode~~ wiring line and the second N-type impurity region of the first semiconductor island and there is no overlap between the second ~~gate electrode~~ wiring line and the second N-type impurity region.

34. (Currently Amended) The method of manufacturing the semiconductor device according to claim 33,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

35. (Currently Amended) The method of manufacturing the semiconductor device according to claim 33,

wherein ~~said~~ the second wiring line and the third ~~gate electrodes~~ wiring line are formed by patterning a second conductive ~~layer~~ film, ~~said~~ the second conductive ~~layer~~ film comprising a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

36. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over ~~said~~ the first ~~gate electrode~~ wiring line with ~~said~~ the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a first channel region therebetween;

forming at least one second N-type impurity region between the first channel region and the first N-type impurity regions, wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in ~~said~~ the first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a second channel region therebetween;

forming a second insulating film over said the first semiconductor island and the second semiconductor ~~islands~~ island; and

forming a second ~~gate electrode~~ wiring line over the first channel region of the first semiconductor island and a third ~~gate electrode~~ wiring line over the second channel region of the second semiconductor island,

wherein there is an overlap between the first ~~gate electrode~~ wiring line and the second N-type impurity region of the first semiconductor island and there is no overlap between the second ~~gate electrode~~ wiring line and the second N-type impurity region, and

wherein the first ~~gate electrode~~ wiring line is electrically connected to the second ~~gate electrode~~ wiring line.

37. (Currently Amended) The method of manufacturing the semiconductor device according to claim 36,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

38. (Currently Amended) The method of manufacturing the semiconductor device according to claim 36,

wherein ~~said~~ the second wiring line and the third ~~gate electrodes~~ wiring line are formed by patterning a second conductive ~~layer~~ film, ~~said~~ the second conductive ~~layer~~ film comprising a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

39. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over ~~said~~ the first ~~gate electrode~~ wiring line with ~~said~~ the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a first channel region therebetween;

forming at least one second N-type impurity region between the first channel region and the first N-type impurity regions, wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in ~~said~~ the first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a second channel region therebetween;

forming a second insulating film over said the first semiconductor island and the second semiconductor ~~islands~~ island; and

forming a second ~~gate electrode~~ wiring line over the first channel region of the first semiconductor island and a third ~~gate electrode~~ wiring line over the second channel region of the second semiconductor island,

wherein the first ~~gate electrode~~ wiring line extends beyond both side edges of the second ~~gate electrode~~ wiring line.

40. (Currently Amended) The method of manufacturing the semiconductor device according to claim 39,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr),titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

41. (Currently Amended) The method of manufacturing the semiconductor device according to claim 39,

wherein ~~said~~ the second wiring line and the third ~~gate~~ electrodes wiring line are formed by patterning a second conductive layer, ~~said~~ the second conductive layer comprising a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

42. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over ~~said~~ the first ~~gate electrode~~ wiring line with ~~said~~

the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a first channel region therebetween;

forming at least one second N-type impurity region between the first channel region and the first N-type impurity regions, wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in ~~said~~ the first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a second channel region therebetween;

forming a second insulating film over ~~said~~ the first semiconductor island and the second semiconductor ~~islands~~ island;

forming a second ~~gate electrode~~ wiring line over the first channel region of the first semiconductor island and a third ~~gate electrode~~ wiring line over the second channel region of the second semiconductor island;

forming a third insulating film over the second wiring line and the third ~~gate electrodes~~ wiring line; and

forming a pixel electrode over the third insulating film,

wherein the first ~~gate electrode~~ wiring line is electrically floating, and

wherein the first ~~gate electrode~~ wiring line extends beyond both side edges of the second ~~gate electrode~~ wiring line.

43. (Currently Amended) The method of manufacturing the semiconductor device according to claim 42,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

44. (Currently Amended) The method of manufacturing the semiconductor device according to claim 42,

wherein ~~said~~ the second wiring line and the third ~~gate electrodes~~ wiring line are formed by patterning a second conductive layer, ~~said~~ the second conductive layer comprising

a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

45. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over ~~said~~ the first ~~gate electrode~~ wiring line with ~~said~~ the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a pair of first N-type impurity regions in the first semiconductor island with a first channel region therebetween;

forming at least one second N-type impurity region between the first channel region and the first N-type impurity regions, wherein a concentration of an N-type impurity in the second N-type impurity region is lower than that in ~~said~~ the first N-type impurity regions;

forming a pair of P-type impurity regions in the second semiconductor island with a second channel region therebetween;

forming a second insulating film over ~~said~~ the first semiconductor island and the second semiconductor ~~islands~~ island; and

forming a second ~~gate electrode~~ wiring line over the first channel region of the first semiconductor island and a third ~~gate electrode~~ wiring line over the second channel region of the second semiconductor island,

wherein the first ~~gate electrode~~ wiring line extends beyond both side edges of the second ~~gate electrode~~ wiring line and is connected to a fixed potential.

46. (Currently Amended) The method of manufacturing the semiconductor device according to claim 45,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr),titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

47. (Currently Amended) The method of manufacturing the semiconductor device according to claim 45,

wherein ~~said~~ the second wiring line and the third ~~gate electrodes~~ wiring line are formed by patterning a second conductive layer, ~~said~~ the second conductive layer comprising a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

48. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive film over a substrate;

patterning ~~said~~ the first conductive film to form at least one first wiring line~~, said first wiring including at least one first gate electrode~~;

forming a first insulating film over ~~said~~ the first wiring line and ~~said~~ the substrate;

forming a first semiconductor island and a second semiconductor island, wherein ~~said~~ the first semiconductor island is located over ~~said~~ the first ~~gate electrode~~ wiring line with ~~said~~ the first insulating film interposed therebetween and ~~said~~ the second semiconductor island does not overlap any portion of the first conductive film;

forming a second insulating film over ~~said~~ the first semiconductor island and the second semiconductor ~~islands~~ island;

forming a second conductive film over the second insulating film;

first etching a portion of the second conductive film to form a second ~~gate electrode~~ wiring line over the first semiconductor island while a portion of the conductive film over the second semiconductor island is not etched, wherein ~~said~~ the first ~~gate electrode~~ wiring line extends beyond side edges of the ~~second gate electrode~~ first semiconductor island;

first introducing an N-type impurity into the first semiconductor island at a first concentration in accordance with a pattern of the second ~~gate electrode~~ wiring line, wherein

~~said~~ the N-type impurity ~~region~~ is prevented from being introduced into the second semiconductor island during the first ~~introduction of~~ introducing the N-type impurity;

second etching another portion of the second conductive film to form a third ~~gate electrode~~ wiring line over the second semiconductor island after the ~~introduction of~~ first introducing of the N-type impurity;

introducing a P-type impurity into the second semiconductor island in accordance with a pattern of the third ~~gate electrode~~ wiring line, wherein ~~said~~ the P-type impurity is prevented from being introduced into the first semiconductor island during the ~~introduction of said~~ introducing the P-type impurity;

forming a first resist mask and a second resist mask, wherein ~~said~~ the first resist mask covers the second ~~gate electrode~~ wiring line and extends beyond side edges of the second ~~gate electrode~~ wiring line, and ~~said~~ the second resist mask is formed over the third ~~gate electrode~~ wiring line;

second introducing an N-type impurity into the first semiconductor island in accordance with ~~said~~ the first resist mask and the second resist mask at a second concentration greater than the first concentration.

49. (Currently Amended) The method of manufacturing the semiconductor device according to claim ~~39~~ 48,

wherein ~~said~~ the first conductive film comprises a material selected from the group consisting of ~~Ta, Cr, Ti, W, Mo and Is~~ tantalum (Ta), chromium (Cr),titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).

50. (Currently Amended) The method of manufacturing the semiconductor device according to claim ~~39~~ 48,

wherein ~~said~~ the second ~~and third gate electrodes are formed by patterning a conductive layer, said~~ conductive layer comprising a material selected from the group consisting of tantalum (Ta), chromium (Cr), titanium (Ti), tungsten (W), molybdenum (Mo), and silicon (Si).